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(54) ELECTRONIC DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide an electronic device in which a member constituting the ceiling part of a cavity is protected against breakageand to provide its manufacturing method.

SOLUTION: The method for manufacturing an electronic device comprises a step for preparing a sacrificial layer for forming a cavity covered with an etching stop layer (silicon nitride film) at least on the upper surface thereofa step for exposing a part of the surface of the sacrificial layer by making at least one first

opening in the etching stop layera step for forming a supporting part of a temporary cavity located below the etching stop layer and the etching stop layer by etching the sacrificial layer through the first openingand a step for forming a final cavity by etching a part of the etching stop layer and forming at least one second opening reaching the temporary cavity in the etching stop layer thereby enlarging the temporary cavity.

CLAIMS

[Claim(s)]

[Claim 1]

A process (a) for which the upper surface prepares at least a sacrifice layer for porosi covered with an etching stop layer

A process (b) which forms 1st at least one opening in said etching stop layer and at which a part of surface of said sacrifice layer for porosi is exposed

A process (c) of forming a temporary cavity in which it is located under said etching stop layer by etching said sacrifice layer for porosi via said 1st openingand a supporter which supports said etching stop layer

A process (d) of forming in said etching stop layer 2nd at least one opening that arrives at said temporary cavity by etching said a part of etching stop layerand forming a cave to which said temporary cavity was expanded

A manufacturing method of a ****** electron device.

[Claim 2]

A manufacturing method of an electron device which includes a statement in claim 1 including a process into which said process (d) etches said at least a part of supporter in which it is located under said 2nd opening via said 2nd opening.

[Claim 3]

The manufacturing method according to claim 1 which performs a process of forming a structure containing a thin film patterned before said process (d) on said etching stop layer.

[Claim 4]
The manufacturing method according to claim 3 formed so that said patterned thin film may cover fields other than a field in which said 2nd opening is formed.
[Claim 5]
A process of depositing on a substrate a film from which said process (a) serves as material of said sacrifice layer for porosi
A process of forming said sacrifice layer for porosi by patterning said film
******the manufacturing method according to claim 1.
[Claim 6]
The manufacturing method according to claim 5 which forms a sacrifice layer for porosi which has a through hole which arrives at the undersurface from the upper surface of said sacrifice layer for porosi.
[Claim 7]
The manufacturing method according to claim 5 or 6 which forms said supporter in a field to which said sacrifice layer for porosi does not exist in said process (c).
[Claim 8]
The manufacturing method according to claim 7 as which said a part of etching stop layer is operated as said supporter.
[Claim 9]
The manufacturing method according to claim 5 which makes said a part of sacrifice layer for porosi remain as said supporter in said process (c).
[Claim 10]
Said process (c) includes a process of etching said sacrifice layer for porosi by wet etching art
The manufacturing method according to claim 2 with which said process (d) includes a process of etching said at least a part of supporter by dry etching technology.
[Claim 11]
The manufacturing method according to claim 1 with which said process (a) includes a process of depositing said etching stop layer on said sacrifice layer for

porosi.

[Claim 12]

The manufacturing method according to claim 1 which prepares a SOI substratecomprising:

A silicon oxide layer which functions as said etching stop layer in said process (a).

A single crystal silicon substrate including a field which functions as said sacrifice layer for porosi.

[Claim 13]

Before performing said process (c)it is a mask which has a pattern which specifies said 2nd openingand a mask on which an inside of said 1st opening is exposed performs a wrap process for said etching stop layer

The manufacturing method according to claim 1 which performs a process of removing said mask after performing said process (d).

[Claim 14]

[after forming said temporary cavitybefore expanding said temporary cavity]

A process of plugging up said 1st opening of said etching stop layer with a thin film

A process of forming a film for sensors on said thin film

A process of patterning said film for sensors

******the manufacturing method according to claim 1.

[Claim 15]

The manufacturing method according to claim 14 which deposits said thin film by chemical vapor deposition.

[Claim 16]

A process of forming an insulator layer for heat absorption on said thin film is included furtherand it is the manufacturing method according to claim 15.

[Claim 17]

The manufacturing method according to claim 16 which includes further a process of forming an insulator layer for protection on said insulator layer for heat

absorption.

[Claim 18]

Said process (a) includes a process of forming diacid-ized silicon in a field selected in the surface of said silicon substrateby oxidizing the surface of a single crystal silicon substrate locally

The manufacturing method according to claim 1 using said at least some of diacid-ized silicon as said sacrifice layer for porosi.

[Claim 19]

The manufacturing method according to claim 18 using said diacid-ized silicon as an insulator layer for isolation.

[Claim 20]

The manufacturing method according to claim 1 in which said sacrifice layer for porosi is a surface portion of a semiconductor substrate.

[Claim 21]

Said process (c)

A process of forming a crevice in said sacrifice layer for porosi from said 1st opening by dry etching technology

A process of etching said crevice isotropic

A manufacturing method given in ****** claim 1.

[Claim 22]

The manufacturing method according to claim 1 which forms said supporter only in the circumference of said temporary cavity in said process (c).

[Claim 23]

The manufacturing method according to claim 1 which forms said supporter in an inside of said temporary cavity in said process (c).

[Claim 24]

A manufacturing method given in the claim 21 for which each cross sectional area forms a pillar more than 10 micrometer^2 as said supporter by or more 3 ten numbers when the total cross sectional area forms said cave more than 1000-micrometer^2.

[Claim 25]

The manufacturing method according to claim 14 which forms a nitride layer as said etching stop layerand forms a diacid-ized silicone film as said thin film.

[Claim 26]

A manufacturing method of the electron device according to claim 4 which includes further a process of forming a cap which intercepts a structure containing said patterned thin film from the outside.

[Claim 27]

A substrate which has at least one cave

A diaphragm-structure object which forms an upper face part of said cave

A thin film which was patterned and was supported with said diaphragm-structure object

It is preparation **********

An electron device which is further provided with at least one hole formed in a field to which said patterned thin film does not exist among said diaphragm-structure objects and with which said hole has reached said cave.

[Claim 28]

The electron device according to claim 27 with which heights which project toward said diaphragm-structure object in just under said hole are formed in an inside of said cave.

[Claim 29]

The electron device according to claim 27 with which a crevice is formed in direction which keeps away from said diaphragm-structure object just under said hole in an inside of said cave.

[Claim 30]

The electron device according to claim 27 which said patterned thin film is a bolometer and functions as an infrared sensor.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

This invention relates to the electron device suitably produced by the manufacturing method of the electron device provided with the infrared sensor etc.and the method concerned.

[0002]

[Description of the Prior Art]

The infrared sensor which has arranged two or more bolometers on a semiconductor substrate is known. The detecting sensitivity of such an infrared sensor will fallif the heat generated in the bolometer by infrared irradiation conducts to a semiconductor substrate. For this reasonit is required to reduce the thermal convectivity between a bolometer and a semiconductor substrate. The patent documents 1 are indicating forming a cave on the surface of a silicon substrate in order to separate a silicon substrate with big calorific capacity from infrared detection objectssuch as a bolometerthermally.

[0003]

Drawing 31 (a) The art indicated in the above-mentioned gazette is explained referring to - (g). According to the method currently indicated by literaturefirstas shown in drawing 31 (a)using LOCOS (Local Oxidation of Silicon) separation technologythe surface of the semiconductor substrate 1001 oxidizes locally and the LOCOS film 1002 is formed.

[0004]

Nextas shown in drawing 31 (b)the silicon nitride layer 1003 and the polysilicon film 1004 are laminated so that the LOCOS film 1002 and the semiconductor substrate 1001 may be covered.

[0005]

Thenas shown in drawing 31 (c)the hole 1005 which penetrates the polysilicon film 1004the silicon nitride layer 1003and the LOCOS film 1002and reaches the

semiconductor substrate 1001 by a photolithography and dry etching technology is formed.

[0006]

Nextas shown in drawing 31 (d)the portion exposed to the wall surface of the hole 1005 among the LOCOS films 1002 is etched into a transverse direction by the wet etching using buffered fluoric acid. At this timethe wall 1007 which is a remaining part of the LOCOS film 1002 is formed between hole 1005 adjoining comrades.

[0007]

Nextas shown in drawing 31 (e)after depositing a thin polysilicon film on the surface of the polysilicon film 1004or the wall surface of the hole 1005this thin polysilicon film and polysilicon film 1004 are oxidizedand the continuous silicon oxide layer 1010 is formed. The hollow part 1011 which is Sorama who each hole was taken up by this processing and closed down is formed.

[0008]

Nextas shown in drawing 31 (f)the patterned conductor film 1012 which functions as an infrared detection object is deposited on the silicon oxide layer 1010. The patterned conductor film 1012 has winding plane shapefor example.

[0009]

Thussince heat transfer from an infrared detection object to the semiconductor substrate 1001 is controlled by forming the hollow part 1011 between the conductor film 1012 and the semiconductor substrate 1001 which are heat primary detecting elementsinfrared detecting sensitivity improves.

[0010]

Nextother methods of forming a hollow part are explained. The infrared sensor which has the cave formed by this method is indicatedfor example to the patent documents 2.

[0011]

Firstas shown in drawing 32 (a) and (b)the silicon oxide layer 301 is deposited on the silicon substrate 300. The silicon oxide layer 301 functions as a lower layer

etching stop layerwhen etching the polysilicon film deposited at the following process.

[0012]

As shown in drawing 33 (a) and (b)after depositing the polysilicon film 302 on the silicon oxide layer 301as shown in drawing 34 (a) and (b)the polysilicon film 302 is patterned. Thusthe patterned polysilicon film 302 functions as a sacrifice layer for porosi.

[0013]

Nextas shown in drawing 35 (a) and (b)after depositing the silicon oxide layer 303 on the polysilicon film 302as shown in drawing 36 (a) and (b)the infrared detection object 304 is formed on the silicon oxide layer 303.

[0014]

As shown in drawing 37 (a) and (b)the silicon oxide layer 305 is deposited so that the infrared detection object 304 may be covered. These silicon oxide layers 303 and 305 function as an upper etching stop layer.

[0015]

Nextas shown in drawing 38 (a) and (b)the silicon oxide layers 303 and 305 are patterned and the opening 306 for porosi is formed. By this opening 306some polysilicon films 302 are exposed. Thenthe silicon oxide layer 303. By making hydrazine flow from the opening 306 formed in 305and etching the polysilicon film 302as shown in drawing 39 (a) and (b)the cave 308 is formed.

[0016]

[Patent documents 1]

JP2001-210877A

[Patent documents 2]

JP05-126643A

[0017]

[Problem(s) to be Solved by the Invention]

According to the method indicated to the above-mentioned patent documents 1the wall 1007 remains in the hollow part 1011 shown in drawing 31 (f). As for

this wall 1007since it has thermal conductivityin order to heighten the effect which provided the caveit is preferred to remove the wall 1007. What is necessary is to lengthen etching time and just to make it not leave the wall 1007 at the process shown in drawing 31 (d)in order to remove the wall 1007. Howeverif the wall 1007 is removed in this stagethe phenomenon in which the silicon nitride layer 1003 and the polysilicon film 1004 will be fractured by the time it forms the structure shown in drawing 31 (f) will be seen. The cause is presumed to be what is depended on the heat stress resulting from the difference of the coefficient of thermal expansion of the silicon nitride layer 1003 and the semiconductor substrate 1001. Namelyannealing for carrying out activity of the impurity doped by the conductor film 1012 which is a polysilicon filmWhen oxidizing thermally the polysilicon film 1004 and the thin polysilicon film on itit is because big heat stress is impressed to the silicon nitride layer 1003 or the silicon oxide layer 1004.

[0018]

For this reasonit is difficult to remove the wall 1007 indicated to the patent documents 1and to form a big cave.

[0019]

On the other handin the method indicated to the patent documents 2since the polysilicon film 302 is removed by drug solutionssuch as hydrazinethe drying process for removing the drug solution in the cave 308 after that becomes indispensable. There is a problem that big stress is occurred and damaged according to such a drying process into the portion (silicon oxide layers 303 and 305) which supports the ceiling part of the cave 308.

[0020]

Made in order that this invention may solve the above-mentioned problemthe main purpose is to provide an electron device which controlled the fracture of the member which constitutes the ceiling part of a caveand a manufacturing method for the same.

[0021]

[Means for Solving the Problem]

A manufacturing method of an electron device of this invention is provided with the following.

A process for which the upper surface prepares at least a sacrifice layer for porosi covered with an etching stop layer (a).

A process (b) which forms 1st at least one opening in said etching stop layer and at which a part of surface of said sacrifice layer for porosi is exposed.

A process (c) of forming a temporary cavity in which it is located under said etching stop layer by etching said sacrifice layer for porosi via said 1st openingand a supporter which supports said etching stop layer.

A process (d) of forming in said etching stop layer 2nd at least one opening that arrives at said temporary cavity by etching said a part of etching stop layerand forming a cave to which said temporary cavity was expanded.

[0022]

In a desirable embodimentsaid process (d) includes a process of etching said at least a part of supporter in which it is located under said 2nd openingvia said 2nd opening.

[0023]

The manufacturing method according to claim 1 which performs a process of forming a structure which contains a thin film patterned before said process (d) in a desirable embodiment on said etching stop layer.

[0024]

In a desirable embodimentsaid patterned thin film is formed so that fields other than a field in which said 2nd opening is formed may be covered.

[0025]

Said process (a) is provided with the following in a desirable embodiment.

A process of depositing a film used as material of said sacrifice layer for porosi on a substrate.

A process of forming said sacrifice layer for porosi by patterning said film.

[0026]

In a desirable embodimenta sacrifice layer for porosi which has a through hole which arrives at the undersurface from the upper surface of said sacrifice layer for porosi is formed.

[0027]

In a desirable embodimentsaid supporter is formed in a field to which said sacrifice layer for porosi does not exist at said process (c).

[0028]

In a desirable embodimentsaid a part of etching stop layer is operated as said supporter.

[0029]

Said a part of sacrifice layer for porosi is made to remain as said supporter at said process (c) in a desirable embodiment.

[0030]

In a desirable embodimentsaid process (c) includes a process into which said process (d) etches said at least a part of supporter by dry etching technology including a process of etching said sacrifice layer for porosi by wet etching art.

[0031]

In a desirable embodimentsaid process (a) includes a process of depositing said etching stop layer on said sacrifice layer for porosi.

[0032]

In a desirable embodimenta SOI substrate provided with a silicon oxide layer which functions as said etching stop layerand a single crystal silicon substrate including a field which functions as said sacrifice layer for porosi is prepared at said process (a).

[0033]

Before performing said process (c) in a desirable embodimentit is a mask which has a pattern which specifies said 2nd openinga mask on which an inside of said 1st opening is exposed performs a wrap process for said etching stop layerand

after performing said process (d)a process of removing said mask is performed.

[0034]

In a desirable embodimentafter forming said temporary cavitybefore expanding said temporary cavitya process of plugging up said 1st opening of said etching stop layer with a thin filma process of forming a film for sensors on said thin filmand a process of patterning said film for sensors are performed.

[0035]

In a desirable embodimentsaid thin film is deposited by chemical vapor deposition.

[0036]

It is an implication further about a process of forming an insulator layer for heat absorption on said thin film in a desirable embodiment.

[0037]

In a desirable embodimenta process of forming an insulator layer for protection on said insulator layer for heat absorption is included further.

[0038]

In a desirable embodimentsaid process (a)Said at least some of diacid-ized silicon is used for a field selected in the surface of said silicon substrate as said sacrifice layer for porosi including a process of forming diacid-ized siliconby oxidizing the surface of a single crystal silicon substrate locally.

[0039]

In a desirable embodimentsaid diacid-ized silicon is used as an insulator layer for isolation.

[0040]

In a desirable embodimentsaid sacrifice layer for porosi is a surface portion of a semiconductor substrate.

[0041]

Said process (c) is provided with the following in a desirable embodiment.

A process of forming a crevice in said sacrifice layer for porosi from said 1st opening by dry etching technology.

A process of etching said crevice isotropic.

[0042]
In a desirable embodimentsaid supporter is formed only in the circumference of said temporary cavity in said process (c).
[0043]
In a desirable embodimentsaid supporter is formed in an inside of said temporary cavity in said process (c).
[0044]
In a desirable embodimentwhen the total cross sectional area forms said cave more than 1000-micrometer^{2}each cross sectional area forms a pillar more than 10-micrometer^2 as said supporter by or more 3 ten numbers.
[0045]
In a desirable embodimenta nitride layer is formed as said etching stop layerand a diacid-ized silicone film is formed as said thin film.
[0046]
In a desirable embodimenta process of forming a cap which intercepts a structure containing said patterned thin film from the outside is included further.
[0047]
A substrate with which an electron device by this invention has at least one cavelt is patterned with a diaphragm-structure object which forms an upper face part of said cavelt is the electron device provided with a thin film supported with said diaphragm-structure objectand it has further at least one hole formed in a field to which said patterned thin film does not exist among said diaphragm-structure objectsand said hole has reached said cave.
[0048]
In a desirable embodimentheights which project toward said diaphragm-structure object in just under said hole are formed in an inside of said cave.
[0049]
In a desirable embodimenta crevice is formed in direction which keeps away from

said diaphragm-structure object just under said hole in an inside of said cave.

[0050]

In a desirable embodimentsaid patterned thin film is a bolometer and functions as an infrared sensor.

[0051]

[Embodiment of the Invention]

Hereafterthe embodiment of this invention is describedreferring to drawings.

[0052]

(A 1st embodiment)

The electron device of this embodiment is an infrared sensor which has an infrared detection part (bolometer).

[0053]

Firstdrawing 1 (a) and (b) is referred to. Drawing 1 (a) and (b) is the sectional view and top view showing the process of forming the sacrifice layer for porosirespectively. In the process shown in these figuresthe field where the surface of the semiconductor substrate 10 was chosen is locally oxidized using publicly known LOCOS separation technology. Since the semiconductor substrate 10 used by this embodiment is a single crystal silicon waferthe insulator layer 11 for caves which consists of silicon oxides (thermal oxidation thing) by this oxidation is formed.

[0054]

Although only the single insulator layer 11 for caves is indicated by the attached drawingtwo or more insulator layers 11 for caves may be simultaneously formed on the one semiconductor substrate 10. Although this specification explains the example which forms one cave in the semiconductor substrate 10 for simplificationif it is a person skilled in the artthe method of forming two or more caves simultaneously will be easily understood from the indication of this specification.

[0055]

In a desirable embodimentvarious circuits (control circuit etc.) required for

operation of a sensor are formed in other fields to which the semiconductor substrate 10 is not illustratedfor example. Such a circuit can be formed on the semiconductor substrate 10 using integrated circuit art. When forming the integrated circuit which contains a transistor etc. as a circuit element on the semiconductor substrate 10it is necessary to separate electrically each MISFET which constitutes an integrated circuit. Such electrical isolation is performed by forming an element isolation insulation film in the semiconductor substrate 10. In order to reduce a manufacturing process numberit is preferred that the process of forming an element isolation insulation film serves as the process of forming the insulator layer 11 for caves.

[0056]

The thickness of the insulator layer 11 for caves in this embodiment is set up from about 0.4 - the range of 1 micrometer of abbreviation. The size of the insulator layer 11 for caves may be chosen in the range from the rectangular shape of 30 micrometers x 30 micrometers to the rectangular shape of 100 micrometers x about 100 micrometers. Howeverthe flat-surface layout of the insulator layer 11 for caves may not be limited to a rectanglebut may be other shape.

[0057]

The insulator layer 11 for caves may be produced by art other than LOCOS separation technology. For examplethe crevice is beforehand formed in the surface of the semiconductor substrate 10and this crevice may also be embedded with the insulator layer deposited by thin film deposition artsuch as a CVD method (trench separation formation art).

[0058]

Nextdrawing 2 (a) and (b) is referred to. Drawing 2 (a) and (b) is the sectional view and top view showing the process of forming the silicon nitride layer which functions on the semiconductor substrate 10 as an etch stopper layerrespectively.

[0059]

In the process shown in drawing 2 (a) and (b)the 200-400-nm-thick silicon nitride

layer 12 is deposited with a CVD method on the semiconductor substrate 10 and the insulator layer 11 for caves. This process holds substrate temperature at 760 **and is performed.

[0060]

Drawing 3 (b) is a top view showing the process of forming the opening for porosi (the 1st opening)and drawing 3 (a) is the IIIa-IIIa line sectional view.

[0061]

In the process shown in drawing 3 (a) and (b)the resist mask (not shown) formed of the photolithography is first formed on the silicon nitride layer 12. This resist mask has a pattern which specifies the opening 15 for porosi which penetrates the silicon nitride layer 12 and the insulator layer 11 for caves. The opening 15 for porosi has an arrangement pattern shown in drawing 3 (b)and reaches the semiconductor substrate 10. Such an opening 15 for porosi is formed by etching the portion which is not covered with the above-mentioned resist mask among the openings 15 for porosiafter etching first the portion which is not covered with the above-mentioned resist mask among the silicon nitride layers 12. These etching is preferably performed by dry etching with high anisotropy. The diameter of the opening 15 is setfor example as about 0.3 micrometer.

[0062]

The twist of the interval of the opening 15 is also relatively large at other places at four places so that drawing 3 (b) may show. At these four placesthe insulator layer 11 for caves will remain at the process of forming the temporary cavity performed to the nextwithout being etched thoroughly.

[0063]

Drawing 4 (b) is a top view showing the process of forming a temporary cavityand drawing 4 (a) is the IVa-IVa line sectional view. In this processwhile etching the insulator layer 11 for caves and forming the temporary cavity 16x by performing wet etching which used buffered fluoric acida supporter is formed with the etching remainder of the insulator layer 11 for caves. This supporter is constituted by the wall 11a which encloses the circumference of the temporary

cavity 16xand the four pillars 11b located in the inside of the temporary cavity 16x. The ceiling part (etch stopper layer) of the temporary cavity 16x is supported by the wall 11a and the pillar 11band faultssuch as fall of a silicon nitride layerare prevented with them.

[0064]

In the process of forming this temporary cavitydirty CHANTO for etching the insulator layer 11 for caves isotropic is supplied to the insulator layer 11 for caves via two or more openings 15 arranged as shown in drawing 3 (b). Since etching advances isotropicnot only the portion just under the opening 15 but the portion just under the field between the adjoining openings 15 is etched among the insulator layers 11 for caves. At four places where the interval of the opening 15 is set up greatly relativelytransverse direction etching from the Mashita portion of the opening 15 advances insufficientlyandas a resultthe etching remainder is formed. The pillar 11b is constituted by this etching remainder. According to this embodimentin the time of etching for forming a temporary cavityif too longthe pillar 11b will become thin and it will disappear eventually. For this reasonit is necessary to adjust the arrangement interval of the opening 15and etching time appropriately.

[0065]

The number and position of the pillar 11b are limited to the number and position of a pillar in this embodimentand do not have an end. The support member which has a size and shape arbitrarily in arbitrary positions can be formed by devising flat-surface layoutssuch as shape of the opening 15and a size.

[0066]

Nextthe process of once plugging up the opening 15 provided in order to form a temporary cavity is performed. Drawing 5 (b) is a top view showing this processand drawing 5 (a) is that Va-Va line sectional view. In this processthe 350-nm-thick silicon oxide layer 20 is deposited on the semiconductor substrate 10 with a CVD method. this silicon oxide layer 20 consists of TEOS(s) preferably -- it forms.

[0067]

The opening 15 for porosi which exists in the silicon nitride layer 12 which is a ceiling part of the temporary cavity 16x is closed by the deposited silicon oxide layer 20. Deposition of the silicon oxide layer 20 is performed by substrate temperature being about 680 **. This temperature is quite low compared with substrate temperature (about 900 **) when performing the process of oxidizing a polysilicon film thermally.

[0068]

In the early stages of the piling process of the silicon oxide layer 20since the whole opening 15 is not plugged upan oxide layer (pars-basilaris-ossis-occipitalis oxide layer 20a) accumulates also on the bottom of the temporary cavity 16x.

[0069]

Nextas shown in drawing 6 (a) and (b)the process of depositing the resistor for bolometers on the silicon oxide layer 20 is performed. Drawing 6 (b) is a top view showing the layout of the patterned resistor for bolometersand drawing 6 (a) is the VIa-VIa line sectional view.

[0070]

In this processafter depositing a 500-nm-thick polysilicon film on the semiconductor substrate 10a polysilicon film is patterned with a photolithography and etching technology. The abbreviated S character-like resistor 21 for bolometers is formed by patterning of a polysilicon filmfor example. This resistor 21 for bolometers will function as an infrared detection part of an infrared sensor. The resistor 21 for bolometers avoids the field in which it is located right above the pillar 11b in the temporary cavity 16xand is formed. In other wordsthe pillar 11b does not exist directly under the resistor 21 for bolometers.

[0071]

Nextthe process of forming an interlayer insulation film as shown in drawing 7 (a) and (b) is performed. Drawing 7 (b) is a top view and drawing 7 (a) is the VIIa-VIIa line sectional view. In this processthe interlayer insulation film 24 which consists of about 700 nm - 1 micrometer-thick BPSG (Boro-Phospho-Silicate

Glass: phosphorus boron glass) is deposited so that the silicon oxide layer 21 and the resistor 21 for bolometers may be covered. This interlayer insulation film 24 functions as an infrared absorption film.

[0072]

Nextas shown in drawing 8 (a) and (b)the process of forming the wiring for bolometers is performed. Drawing 8 (b) is a top view showing the layout of wiringand drawing 8 (a) is the VIIIa-VIIIa line sectional view.

[0073]

In this processfirstby a photolithography and dry etching technologythe interlayer insulation film 24 is penetrated and two holes which arrive at the both ends of the resistor 21 for bolometers are formed. Thena hole is filled up with W (tungsten) and the two plugs 26 connected to the both ends of the resistor 21 for bolometersrespectively are formed. After depositing an Al alloy film on the interlayer insulation film 24an Al alloy film is patterned and the wiring 25 connected to each plug 26respectively is formed. This wiring 25 electrically connects the picture element part and peripheral circuit where a bolometer is arranged. It is with the time of the resistor 21 being irradiated by infrared raysand the time of infrared rays not glaringand since resistance of the resistor 21 changesif a resistance change is detected based on the current which flows through the wiring 25it is possible to detect the amount of infrared irradiationso that it may explain later.

[0074]

Nextthe process of forming a passivation film is performed. Drawing 9 (b) is a top view in the state where the passivation film was formedand drawing 9 (a) is a sectional view in the IXa-IXa line. this process -- the interlayer insulation film 24 and the wiring 25 -- ** -- the passivation film 27 which consists of silicon nitride layers is deposited like. The passivation film 27 also plays a role of an infrared absorption layer while being an insulator layer for protection. The growing temperature of the passivation film 27 is about 400 **.

[0075]

Nextthe process of forming a final cave is performed. Drawing 10 (b) is a top view showing the state where the cave was formedand drawing 10 (a) is the Xa-Xa line sectional view. In this processthe portion located above the pillar 11b among the passivation film 27the interlayer insulation film 24the silicon oxide layer 20and the silicon nitride layer 12 is etched by a photolithography and dry etching technologyand the hole (the 2nd opening) 28 is formed. This hole 28 also etches the pillar 11b in the temporary cavity 16x from the upper part. this process -- the slack of the pillar 11b from which the upper part is removed at least that there is nothing -- the last cave 16A which capacity expanded rather than the temporary cavity is formed of things. In the example shown in drawing 10 (a)the whole pillar 11b is removed and a part of pars-basilaris-ossis-occipitalis oxide layer 20a is removed further.

[0076]

At this embodimentat the process shown in drawing 4 (a) and (b)although the pillar 11b is formedit may replace with the pillar 11b and the wall (supporter) which has a layout so that the resistor 21 for bolometers may not overlap may be formed. When such a wall is formedit is a process shown in drawing 10 (a) and (b)the hole 28 will be formed above a walland a wall will remove a part (preferably all) at least by etching.

[0077]

Inside **** and the last cave 16Aat least a part of supporterssuch as a pillar and a wallare removed at the manufacturing method of this embodiment. For this reasonsince the whole supporter is removed or connection to a supporter and an etching stop layer is cutthe thermal conductance between the resistor 21 for bolometers and a silicon substrate can be reducedand improvement in infrared detecting sensitivity or detection precision can be aimed at.

[0078]

At this embodimentthe CVD oxide layer has closed the opening 15 for porosi of the silicon nitride layer 12 which functions as an etching stopper. When oxidation of polysilicon closes the opening 15there is a possibility that hot processing may

be neededdistortion may be given to each member of a ceiling partand destruction of a ceiling part may arisebut according to this embodimentsince such high temperature processing becomes unnecessaryit is desirable. When forming a transistor etc. apart from especially an infrared detection part on the semiconductor substrate 10high temperature heat treatment has a possibility of having an adverse effect on transistor characteristics.

[0079]

In this embodimentalthough the LOCOS film was used as a foundation layer for the porosiit may replace with a LOCOS film and the insulator layer for isolation formed using trench separation artsuch as STI (Shallow Trench Isolation)may be used.

[0080]

As the resistor 21 for bolometersnot only polysilicon but TiTiOPtVO$_x$etc. can be used. Resistance changes in connection with a rise in heat when infrared rays are receivedand such materials can be used as a resistance change type infrared detection part (bolometer).

[0081]

As for the thickness with the passivation film 27 and the interlayer insulation film 24in the case of the infrared sensor of this embodimentit is preferred that it is the 1-micrometer or more range of 2 micrometers or less (for examplearound 1.6 micrometers). The rate of infrared absorption can be highly maintained as the thickness of these films is 1 micrometers or moreand calorific capacity can be prevented from becoming it excessive that membranous thickness is 2 micrometers or less.

[0082]

Since high temperature processing is performed in two or more processes when using a silicon processin order to form the bolometer which is an infrared detection partthe internal stress according to the rate-of-expansion difference (contraction difference) of the material which constitutes each part of a bolometer occurs. For this reasonthere are the following problems in conventional

technology.

[0083]

(1) If the number or cross sectional area of a pillar for supporting the ceiling part of a cave is made smallthere is a possibility that the intensity of the ceiling part of a cave may fall and a cave may be damaged by a manufacturing process.

[0084]

(2) If the number or cross sectional area of a pillar for supporting the ceiling part of a cave is enlargedheat insulation between an infrared detection part (bolometer) and the substrate of the lower part will be insufficientand sensor sensitivity will worsen.

[0085]

Hereafterthe above-mentioned problem is explained in detail taking the case of breakage by the tensile stress after growth of a silicon nitride layer. Drawing 11 (a) - (d) is a perspective view for explaining the fault of the manufacturing process of the infrared sensor by the manufacturing method of the comparative example over this embodiment. Drawing 12 (a) - (c) is a perspective view for explaining the advantage of the manufacturing process of the infrared sensor of this embodiment.

[0086]

If substrate temperature is returned to ordinary temperature after depositing a silicon nitride layer on the insulator layer for caves by CVD as shown in drawing 11 (a)a substrate will curve upit will pull to a silicon nitride layerand distortion will arise. Drawing 11 (a) shows the state in the process shown in drawing 2 (a) and (b). The causes of this stress are a difference of the coefficient of thermal expansion (heat shrinkage rate) of a silicon nitride layer and a silicon substratea structure defect produced depending on a growing conditionetc. According to a certain literature (Maruzen Co.Ltd. applied physics data book p.528)the size of the tensile stress of the silicon nitride layer at this time is 10^{-10} (dyn/cm^2)when a silicon nitride layer is depositedfor example on a silicon substrateand it is a general very big value.

[0087]

Nextby dry etchingas shown in drawing 11 (b)if a hole is formed in a silicon nitride layer and the insulator layer for cavesa silicon nitride layer will be in the state where it is pulled further. Drawing 11 (b) shows the state in the process shown in drawing 3 (a) and (b).

[0088]

Nextas shown in drawing 11 (c)in order to raise the sensitivity of an infrared sensorsuppose that the last cave was formed by wet etching without making a pillar and a wall remain. If the insulator layer for caves which consists of silicon oxide layers is thoroughly removed at this time and the last cave is formedin order that stress may concentrate on a silicon nitride layera silicon nitride layer will fracture selectively. As a resultas shown in drawing 11 (d)there is a possibility that a silicon nitride layer may fall in the last cave.

[0089]

According to the manufacturing method of this embodimentto itas shown in drawing 12 (a)unlike the process shown in drawing 11 (c)the temporary cavity where the pillar remains is first formed by wet etching from the state shown in drawing 11 (b) (refer to drawing 4 (a) and (b)). In this statesince the silicon nitride layer is supported by the pillara fracture and fall of a silicon nitride layer as shown in drawing 11 (c) and (d) can be controlled effectively.

[0090]

And as shown in drawing 12 (b)after a TEOS film closes the ceiling part of a temporary cavityan interlayer insulation film and a passivation film are deposited (refer to drawing 5 (a)(b)and drawing 6 (a) and (b)). A silicon nitride layer will be strengthened at this time with a TEOS filman interlayer insulation filmand a passivation film. Although the resistor for bolometers is formed between the TEOS film and the interlayer insulation filmthe graphic display of the resistor for bolometers is omitted in drawing 12 (b).

[0091]

Thenas shown in drawing 12 (c)the last cave is formed by removal of the pillar of

a temporary cavity (refer to drawing 10 (a) and (b)). Although wiring and a passivation film are formed on the interlayer insulation filmthe graphic display of wiring is omitted in drawing 12 (c).

[0092]

Thereforean infrared sensor with high detection sensitivity and detecting accuracy can be formed with the manufacturing method of this embodimentpreventing the fracture and fall of a silicon nitride layer which are etching stoppers and are also the skeletons of the ceiling part of a cave.

[0093]

(A 2nd embodiment)

Also in this embodimenta process until it forms the last cave is as having explained with reference to drawing 1 (a) in a 1st embodiment - drawing 10 (b).

[0094]

Drawing 13 (b) is a top view immediately after performing the process of forming the last cave in this embodimentand drawing 13 (a) is the XIIIa-XIIIa line sectional view.

[0095]

According to this embodimentthe position and shape of the 2nd opening which are formed in the passivation film 27the interlayer insulation film 24and the silicon nitride layer 12 change from the position and shape of the 2nd opening in a 1st embodiment with a photolithography and dry etching. More specifically by this embodimentthe hole 30 is formed as the 2nd opening on the side wall part 11a which encloses the temporary cavity 16x. And via this hole 30at least a part of side wall part 11a is etchedand the last cave to which the temporary cavity was expanded is formed.

[0096]

Although the pillar 11b remains by this processwithout being etcheda part of side wall part 11a is etched from the upper partand it changes to the side wall part 11c with narrower width. As a resultthe last cave 16B with a larger cross sectional area than a temporary cavity will be formed. A part of pars-basilaris-

ossis-occipitalis oxide layer 20a on the bottom of the last cave 16B is removed by the above-mentioned etching process.

[0097]

In a 1st embodimentall the pillars in the last cave 16A are removed. Howeverwhen the area of the last cave 16A is large in comparisona possibility that the member which constitutes the ceiling part of the last cave 16A may fracture and fall arises. According to this embodimentimprovement in the sensitivity of infrared detection and accuracy is aimed at by removing a part of side wall part 11aleaving the pillar 11b.

[0098]

Since the silicon oxide layer 20 which plugs up the opening for porosi of the silicon nitride layer 12 is formed with the CVD method also in this embodimentLike a 1st embodimentwithout giving big heat distortion to the ceiling part of a cavea process can be advanced and the same effect as a 1st embodiment can be demonstrated.

[0099]

When the cross sectional area of the last cave is more than 1000-micrometer^{2}and a cross sectional area leaves the pillar more than 10-micrometer^2 to an inside by or more 2 ten or less numbersthe fracture of the ceiling part of a caveetc. can be prevented certainly.

[0100]

On the contraryeven if it removes the pillar 11bwhen destruction of a ceiling part does not become a problemafter forming the hole 28 formed by a 1st embodiment with the above-mentioned hole 30a part or all of not only the wall 11a but the pillar 11b may be etched.

[0101]

(A 3rd embodiment)

Nexta 3rd embodiment of this invention is described. According to this embodimenta silicon substrate is used as a foundation layer (sacrifice layer for porosi) for forming a cave.

[0102]

Firstas shown in drawing 14 (a) and (b)the process of forming the silicon nitride layer 42 on the substrate 40 is performed. Drawing 14 (b) is a top view showing the substrate 40 in the state where the silicon nitride layer 42 was formedand drawing 14 (a) is the sectional view.

[0103]

In this processthe 200-400-nm-thick silicon nitride layer 42 is deposited with a CVD method on the silicon substrate 40 held at 760 **. The silicon nitride layer 42 functions as an etching stop layer.

[0104]

Nextas shown in drawing 15 (a) and (b)the process of forming the opening 45 in the silicon nitride layer 42 is performed. Drawing 15 (b) is a top view showing arrangement of the opening 45and drawing 15 (a) is the XVa-XVa line sectional view.

[0105]

In this processthe opening 45 for porosi is formed in the silicon nitride layer 42 by performing dry etching using the resist mask (not shown) formed by photolithography technique. In the example shown in drawing 15 (b)the nine openings 45 of three lines x three rows are formed. The interval of the opening 45 in the line of the three openings 45 located in a line with the transverse direction compared with the interval of the opening 45 in the sequence of the three openings 45 perpendicularly located in a line is large.

[0106]

Nextas shown in drawing 16 (a) and (b)the process of forming a temporary cavity is performed. Drawing 16 (b) is a top view of the stage where the temporary cavity was formedand drawing 16 (a) is the XVIa-XVIa line sectional view.

[0107]

In this processa part of silicon substrate 40 is removed by performing wet etching which used alkali system etching reagentssuch as KOH and hydrazine. This etching advances isotropic from the field exposed via the opening 46 among the

surfaces of the silicon substrate 40. Since isotropic wet etching advances not only in a depth direction but in a transverse directionit is etched from the opening 45 of both sides in the field located between the adjoining openings 45 for porosi. Thereforeas shown in drawing 16 (b)the crevice formed by etching connects in the narrow portion of an intervalbut the portion which is not etched remains in the large portion of an interval.

[0108]

In this wayas shown in drawing 16 (a) and (b)while two or more temporary cavities 46x are formedthe wall 40a which is the remainder of the silicon substrate 40 is formed between each temporary cavity 46x.

[0109]

Although temporary cavity 46x on a par with the lengthwise direction of the figure is connected mutually and temporary cavity 46x on a par with the transverse direction of the figure is not open for free passage in the example of drawing 16 (b)the gestalt of the temporary cavity 46x is not limited to such an example. Two or more temporary cavities 46x may be isolated mutuallyand may each-other be partly open for free passage. The temporary cavity 46x free passage of all may be done. The gestalt of the temporary cavity 46x can be freely designed to the shape of the opening 45 for porosia sizearrangementetc.and can be changed also by the conditions of wet etching.

[0110]

In this embodimentit is important to make the wall 40a which functions as a supporter of an etching stop layer and prevents collapse of a temporary cavity remain. For this reasonwhen performing etching for forming the temporary cavity 46xit is necessary to adjust an etching condition so that one continuous big cave without a pillar or a wall may not be formed.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1](a) And (b) is the sectional view and top view showing the process of forming the insulator layer for caves among the manufacturing processes of the bolometer concerning a 1st embodimentrespectively.

[Drawing 2](a) And (b) is the sectional view and top view showing the process of forming a silicon nitride layer on a substraterespectively.

[Drawing 3](a) And (b) is the sectional view and top view in the IIIa-IIIa line which shows the process of forming the opening for porosirespectively.

[Drawing 4](a)(b)and (c) are drawing of longitudinal section in the IVa-IVa line which shows the process of forming a temporary cavityrespectivelya top viewand a partial cross-sectional view.

[Drawing 5](a) And (b) is the sectional view and top view in the Va-Va line which shows the process of once taking up a temporary cavityrespectively.

[Drawing 6](a) And (b) is the sectional view and top view in the VIa-VIa line which shows the process of forming the resistor for bolometers.

[Drawing 7](a) And (b) is the sectional view and top view in the VIIa-VIIa line which shows the process of forming an interlayer insulation filmrespectively.

[Drawing 8](a) And (b) is the sectional view and top view in the VIIIa-VIIIa line which shows the process of forming the wiring for bolometersrespectively.

[Drawing 9](a) And (b) is the sectional view and top view in the IXa-IXa line which shows the process of forming a passivation filmrespectively.

[Drawing 10](a) And (b) is the sectional view and top view in the Xa-Xa line which shows the process of forming the last caverespectively.

[Drawing 11](a) - (d) is a perspective view for explaining the fault of the manufacturing process of the infrared sensor by the manufacturing method of the comparative example over a 1st embodiment.

[Drawing 12](a) - (c) is a perspective view for explaining the advantage of the manufacturing process of the infrared sensor of a 1st embodiment.

[Drawing 13](a) And (b) is the sectional view and top view in the XIIIa-XIIIa line which shows the process of forming the last cave in a 2nd

embodimentrespectively.

[Drawing 14](a) And (b) is the sectional view and top view showing the process of forming a silicon nitride layer on the substrate in a 3rd embodimentrespectively.

[Drawing 15](a) And (b) is the sectional view and top view in the XVa-XVa line which shows the process of forming an opening in a silicon nitride layerrespectively.

[Drawing 16](a) And (b) is drawing of longitudinal section and the top view in the XVIa-XVIa line which shows the process of forming a temporary cavityrespectively.

[Drawing 17](a) And (b) is the sectional view and top view in the XVIIa-XVIIa line which shows the process of once taking up a temporary cavityrespectively.

[Drawing 18](a) And (b) is the sectional view and top view in the XVIIIa-XVIIIa line which shows the process of forming the last cave.

[Drawing 19](a) And (b) is the sectional view and electric diagram of an infrared sensor concerning a 4th embodiment.

[Drawing 20](a) - (e) is a sectional view showing the formation method of a cap body used for the electron device of a 4th embodiment.

[Drawing 21]It is a sectional view showing roughly the composition of the device used for sticking by pressure in a 4th embodiment.

[Drawing 22]It is an electric diagram for explaining the composition of the infrared ray area sensor concerning a 5th embodiment.

[Drawing 23]It is a timing chart which shows the control method of the infrared ray area sensor of a 5th embodiment.

[Drawing 24]It is a sectional view showing the structure of the infrared sensor of a 5th embodiment roughly.

[Drawing 25]It is a sectional view showing the structure of the infrared sensor of a 6th embodiment roughly.

[Drawing 26]It is a sectional view showing the structure of the infrared sensor of the modification of a 6th embodiment roughly.

[Drawing 27]It is a perspective view showing the structure of the infrared

detection part of the pyro infrared sensor concerning a 7th embodiment.

[Drawing 28]It is a sectional view of the infrared detection part of the pyro infrared sensor concerning a 7th embodiment.

[Drawing 29]It is a top view of the infrared detection part of the pyro infrared sensor concerning a 7th embodiment.

[Drawing 30]It is an electric diagram showing the control circuit of the pyro infrared sensor of a 7th embodiment.

[Drawing 31](a) - (f) is a sectional view near an infrared detection part showing the manufacturing process of the semiconductor device for the conventional infrared imaging apparatus currently indicated by the patent documents 1.

[Drawing 32](a) is a top view showing other conventional technologiesand (b) is the XXXIIb-XXXIIb line sectional view.

[Drawing 33](a) is a top view showing other conventional technologiesand (b) is the XXXIIIb-XXXIIIb line sectional view.

[Drawing 34](a) is a top view showing other conventional technologiesand (b) is the XXXIVb-XXXIVb line sectional view.

[Drawing 35](a) is a top view showing other conventional technologiesand (b) is the XXXVb-XXXVb line sectional view.

[Drawing 36](a) is a top view showing other conventional technologiesand (b) is the XXXVIb-XXXVIb line sectional view.

[Drawing 37](a) is a top view showing other conventional technologiesand (b) is the XXXVIIb-XXXVIIb line sectional view.

[Drawing 38](a) is a top view showing other conventional technologiesand (b) is the XXXVIIIb-XXXVIIIb line sectional view.

[Drawing 39](a) is a top view showing other conventional technologiesand (b) is the XXXIXb-XXXIXb line sectional view.

[Drawing 40](a) is a top view showing an 8th embodimentand (b) is the XLb-XLb line sectional view.

[Drawing 41](a) is a top view showing an 8th embodimentand (b) is the XLIb-XLIb line sectional view.

[Drawing 42](a) is a top view showing an 8th embodimentand (b) is the XLIIb-XLIIb line sectional view.

[Drawing 43](a) is a top view showing an 8th embodimentand (b) is the XLIIIb-XLIIIb line sectional view.

[Drawing 44](a) is a top view showing an 8th embodimentand (b) is the XLIVb-XLIVb line sectional view.

[Drawing 45](a) is a top view showing an 8th embodimentand (b) is the XLVb-XLVb line sectional view.

[Drawing 46](a) is a top view showing an 8th embodimentand (b) is the XLVIb-XLVIb line sectional view.

[Drawing 47](a) is a top view showing an 8th embodimentand (b) is the XLVIIb-XLVIIb line sectional view.

[Drawing 48](a) is a top view showing an 8th embodimentand (b-1) and (b-2) are the XLVIIIb-XLVIIIb line sectional view.

[Drawing 49](a) is a top view showing a 9th embodimentand (b) is the ILb-ILb line sectional view.

[Drawing 50](a) is a top view showing a 9th embodimentand (b) is the Lb-Vb line sectional view.

[Drawing 51](a) is a top view showing a 9th embodiment(b) is the LIb-LIb line sectional viewand (c) is a LIc-LIc line sectional view.

[Drawing 52](a) is a top view showing a 9th embodiment(b) is the LIIb-LIIb line sectional viewand (c) is a LIc-LIc line sectional view.

[Drawing 53](a) is a top view showing a 10th embodimentand (b) is the LIIIb-LIIIb line sectional view.

[Drawing 54](a) is a top view showing a 10th embodimentand (b) is the LIVb-LIVb line sectional view.

[Drawing 55](a) is a top view showing an 8th embodimentand (b) is the LVb-LVb line sectional view.

[Drawing 56](a) is a top view showing a 10th embodimentand (b) is the LVIb-LVIb line sectional view.

[Drawing 57](a) is a top view showing a 10th embodimentand (b) is the LVIIb-LVIIb line sectional view.

[Drawing 58](a) is a top view showing an 8th embodimentand (b) is the LVIIIb-LVIIIb line sectional view.

[Drawing 59](a) is a top view showing an 8th embodimentand (b) is the LIXb-LIXb line sectional view.

[Drawing 60](a) is a top view showing an 8th embodimentand (b) is the LXb-LXb line sectional view.

[Drawing 61](a) is a top view showing an 8th embodimentand (b) is the LXIb-LXIb line sectional view.

[Description of Notations]

10 Silicon substrate

11 The insulator layer for porosi (sacrifice layer: foundation layer)

11a Side wall part (support member)

11b Pillar (support member)

12 Silicon nitride layer (etching stop layer)

15 The opening for porosi

16x Temporary cavity

16A The last cave

20 Silicon oxide layer (chemical-vapor-phase-growth film)

21 The resistor for bolometers (film for sensors)

24 Interlayer insulation film (heat-absorbing film)

25 Wiring

26 Plug